

Soft Switched AC-Link AC/AC and AC/DC Buck-Boost Converter

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Abstract— A novel soft switched ac-link buck-boost converter for medium and high power ac-ac and ac-dc applications is proposed. The proposed configuration uses two bi-directional switches per leg of the converter resulting in 12 bi-directional switches for a three-phase to three-phase topology. Power transfer from input to output is accomplished via a link inductor which is first charged from the input phases, then discharged to the output phases with a precisely controllable current PWM technique. Capacitance in parallel with the link inductor produces low turn-off losses. Turn-on is always at zero voltage as each switch swings from reverse to forward bias. Reverse recovery is with low di/dt and also is buffered due to the link capacitance. The soft switching nature of the converter permits use of slower switches with high link frequencies. Converter operation is bi-directional and supports any input or output power factor or voltage, within the current and voltage capacity of the switches. Simulation results showing converter operation under different conditions are presented along with loss calculations. The topology is expected to offer relatively low weight, compact and efficient power converters and motor drives.

I. INTRODUCTION

Conventional variable frequency drives employing dc voltage or current links between the input and output stages have significant limitations resulting from high switching losses and device stress during switching intervals. These restrict practical switching frequencies and reduce semiconductor utilization. Difficulties with input harmonics, output dV/dt and over voltage, EMI/RFI, tripping with voltage sags in the case of rectifier input drives, and other problems diminish the economic competitiveness of these drives. Add-ons such as harmonic filters are available to mitigate these problems but may result in doubling or tripling the total costs and losses, with accompanying large increases in volume and weight.

The last two decades have seen investigations of high frequency link converters as possible improved alternatives. High frequency link dc-dc converters [1]-[4], high frequency link ac-dc converters [5] and the high frequency link dc-ac inverters [6]-[8] have been investigated earlier.

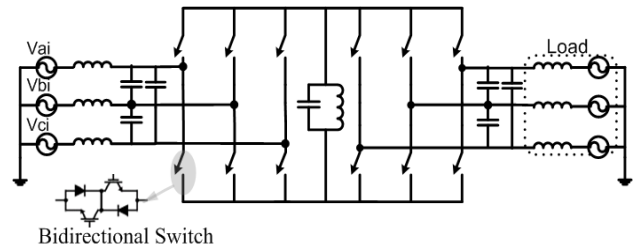


Figure 1. Schematic of proposed topology

However, the research on ac-ac converters are mainly limited to the thyristor phase controlled cycloconverters [9] and matrix converters [10]. These have not found large scale industrial acceptance owing to drawbacks such as complexity of control, limited output voltage capability (86% of input voltage), frequency limitations, and/or reduced efficiency because of hard switching. Reference [5] reported a topology that provided one-step bidirectional power conversion for different kinds of loads/sources. This configuration used twelve bidirectional switches and employed Pulse Density Modulation (PDM) as a means to control the currents. The use of PDM reduces the system response and degrades power quality because of usage of integral pulses of currents. Topologies that make use of twelve unidirectional switches, by providing a dc offset to the dc link, have also been suggested. Reference [11] proposes a topology with twelve unidirectional switches, without the dc offset. However, it is limited in operation response due to its inability to supply output current at low voltages or power factors, at link frequencies sufficiently high to avoid input/output filter resonances. Also, there is a large dead time due to the resonant 'fly back' which reduces the power capability by about 30%. This largely negates its advantage of using a lower numbers of switches compared to the proposed topology.

This paper presents continued work on a new ac-link converter that overcomes the aforementioned drawbacks. The reader may refer [12] as a predecessor to the work presented in this paper. In this paper, simulation results from the inherently bidirectional and multifunctional converter for 2MW medium voltage applications are presented along with detailed loss and efficiency calculations.

A true ac link primarily comprised of a low reactance inductor transfers energy in high frequency current pulses from the input to the output, with low per unit line capacitance filtering the pulses. The resulting low amplitude, high frequency voltage ripple on both input and output requires little if any additional line inductance to achieve less than 3% harmonics, making this topology inherently IEEE 519 compliant. A small link capacitance, in parallel with the link inductor, provides for zero voltage switching (ZVS) at turn-off.

The reverse blocking switches undergo very soft reverse recovery and have zero-voltage turn-on. The resulting low switching losses as predicted by our models shown below promise to allow even medium voltage converters of this type to operate at full power at link frequencies of over 3.5 kHz., and, as there are two power transfers per link cycle, the input and output voltage ripple is twice the link frequency or 7 kHz for a 3.5 kHz link. This high frequency current pulse operation on lightly buffered input and outputs, made possible by low-loss soft switching and accompanying low EMI, results in low per unit component ratings, which in turn enables the claimed high power densities.

High frequency operation also produces very low harmonics, with soft switching producing high efficiency despite the high frequency operation. The high frequency link also allows operation with higher frequency ac, such as 250 Hz as may be encountered with flywheel energy storage. Inputs never directly connect to the outputs and hence there is inherent isolation between the two, which avoids any common mode voltage and enables grounding of both input and output neutral points. Full I/O galvanic isolation may be provided by a split winding version of the link inductor. Symmetrical arrangement of the power circuit also provides fully regenerative operation together with buck-boost capability.

It may be noted that while at least one of the resonant link topologies bears a superficial resemblance to the proposed topology [13], they transfer power around the link, not through it, as with this topology, and typically use discrete pulse modulation which introduces high levels of low frequency harmonics. Peak link voltages at twice the peak line-to-line voltage require high voltage rating switches, and the large reactive power of the link adds to the converter's losses.

Another topology also described as using an AC link [14] may be better considered as a resonant DC link, in that the link is first resonantly charged from the input while starting at zero volts, then resonantly discharged to the output, using two separate inductors and a central capacitor. Link operation may be considered quasi-static, in that the output operation may be indefinitely delayed after the input operation is complete, which is a means of controlling power throughput in that configuration. Unlike the proposed topology, this quasi-static link topology has significant limitations regarding buck-boost operations. Also, the link of the proposed topology is fully AC, with no DC offset in any mode, and the link always oscillates.

II. PROPOSED TOPOLOGY

Figure 1 shows a schematic of the proposed topology. Each leg of the converter is made of 2 bidirectional

switches, realized by anti-series IGBT/diodes' for the 15 kW prototype that is nearing completion. SGCTs or IGBTs rated to 5500 V or more could be used for medium voltage (2300 VAC and up) high power applications. Series operation of switches as needed for voltages greater than 2700 VAC is made simple by the soft switching.

The converter operates by charging the link from the inputs and then discharging the stored energy to the output. The converter is fed with the output current references. The link is charged to an amount which makes the discharging current exactly meet these references. Charging and discharging take place separately, hence, an estimate of how much the link needs to be charged to supply the output correctly is required. The controller handles this by translating the output references to input references. The input reference is derived by the simple equation that

$$\text{Input Power} = \text{Output Power} + \text{Losses}$$

Figure 2 shows a block diagram of how the system works. RMS values of the output reference currents, output and input voltages are used to determine the RMS of the input currents for an ideal converter. A loss component is added to this from the loss estimator to get the exact input command currents. The instantaneous value of the output reference commands could be phase shifted with respect to the output voltages as the load demands. Normally, the instantaneous values of the input current commands are in phase or are phase adjusted with respect to the input voltages so as to achieve unity power factor, but non-unity power factor may also be achieved if required. Figure 3 shows the first four modes of operation while Figure 4 shows the relevant waveforms during all modes of operation (16 in total). The input phase selection block in Figure 2 selects the phase pairs that will charge the link during modes I and III. Normally, for a current command that is in phase with the voltages, these phase pairs are the ones having the highest and the second highest instantaneous voltages respectively.

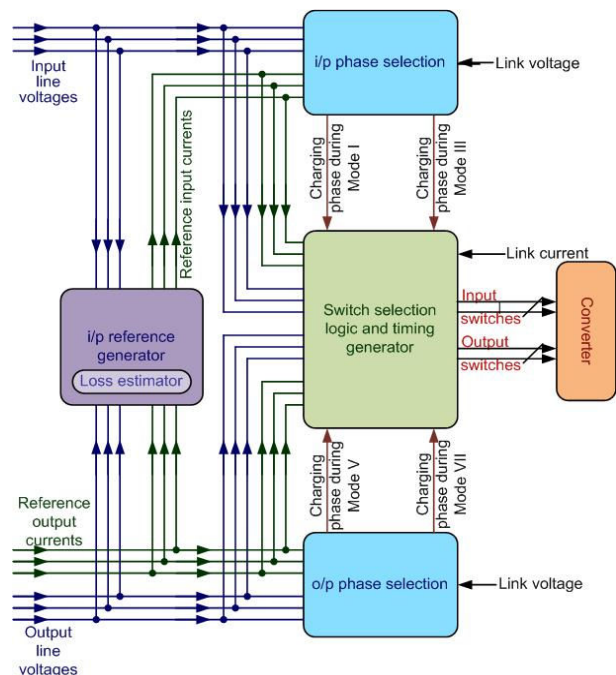


Figure 2. Block diagram showing converter operating principle

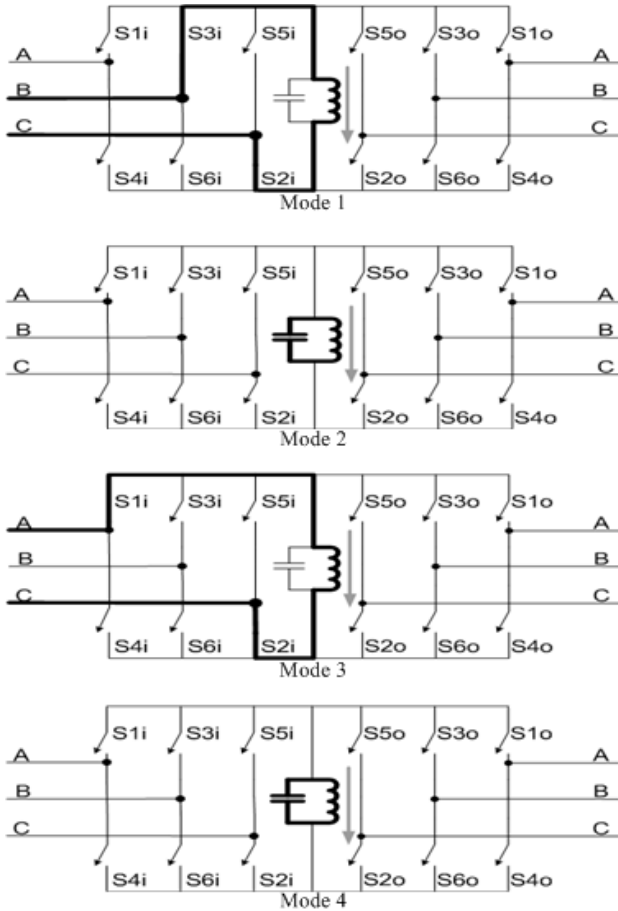


Figure 3. Modes I-IV of operation

Based on the direction of charging of the link required (positive or negative), switches are turned on to allow charging from the selected input phases. Charging takes place till the input reference currents for the phases are met accurately over a charging cycle. In Figure 4, lines BC and AC charge the link during modes I and III. Charging stops in mode I when the reference current of phase B is met, while the same occurs in mode III when the reference current of phase A is met. Between modes I and III, is mode II, where all switches are turned off, to allow the link to partially resonate. Partial resonant modes occur after every charge or discharge. During the partial resonant periods, the link resonates till its voltage becomes equal to the voltage of the input/output phase pair that is to be turned on next. This ensures equal voltages on either side of the switches at the instant of switching to produce zero voltage turn on.

Once the link is charged to the required extent, it swings to the outputs to allow discharging. Output phases to discharge to are also chosen similar to the inputs. While having reference currents that are out of phase with the voltages, the charging/discharging sequence is chosen such that there are minimal partial resonance periods, while allowing the references to be met. Modes 9 through 16 are similar to modes 1 to 8, except that the link current direction is reversed. Reference [12] gives a more complete and detailed explanation of the working of the converter.

III. POWER AND LOSS CALCULATIONS

Knowing the voltage and current levels for the converter, a nominal link frequency is chosen based on the switching characteristics of commercially available switches and stray inductances. The chosen link frequency, the peak voltage and the peak current set the link inductance value. Link capacitance is chosen so as to limit the total partial resonant periods to about 5% of the link cycle. For the 2MW, 2300V medium voltage drive simulated, the parameters are chosen as in Table 1.

Since all power is transferred through the link inductor power transferred through the converter is simply the power through the inductor, with two power transfers per link cycle. This can be calculated with knowledge of the

TABLE I.
CONVERTER PARAMETERS

Link frequency, f_l	3500 Hz
Peak link current, I_p	2800 A
Link inductance, L_l	73 μ H
Link capacitance	5.75 μ F
Input line inductance	200 μ H
Output line inductance	600 μ H

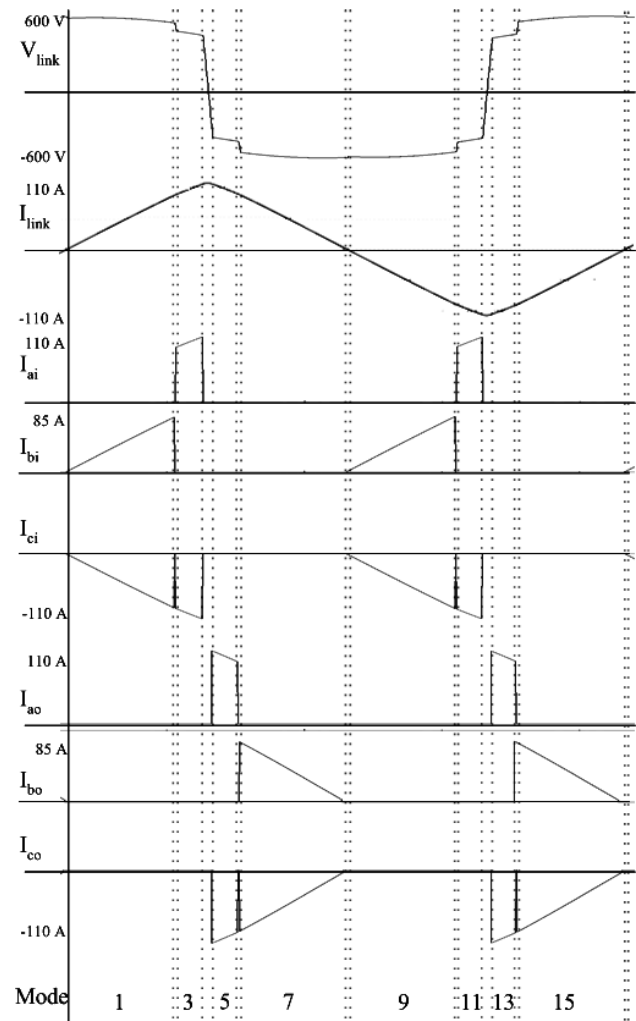


Figure 4. Relevant waveforms during link cycle

link frequency, the link inductance and the peak inductor current, given by:

$$P = f_L L_L I_p^2 = 3500 * 73\mu * 2800^2 = 2003 \text{ kW} \quad (1)$$

A. Conduction Losses

Calculation of conduction losses is also straightforward. Examination of the operating modes shows that only two switches conduct at any given time (which explains the inherent input-output isolation), and the current is triangular, always linearly increasing or decreasing (ignoring the brief partial resonant periods). Conduction loss, given by the switch threshold voltage and the average current, and the switch incremental resistance with the rms current during the conduction interval, is:

$$\begin{aligned} P &= 2 * (V_{sw} * \frac{I_p}{2} + R_{sw} * (0.577 * I_{sw\text{peak}}))^2 \\ &= 2 * (3.5 * \frac{2800}{2} + 0.0036 * (0.577 * 2800))^2 \\ &= 28.59 \text{ kW} (1.42 \%) \end{aligned} \quad (2)$$

where, V_{sw} is the switch threshold voltage, and R_{sw} is the switch resistance. This analysis assumes that the higher conduction loss fast recovery diodes in the module are replaced with low loss rectifier grade diodes, as fast recovery is not needed. For example, for normal motoring operation, reverse recovery does not occur at all until $\frac{1}{4}$ of a link cycle ($71 \mu\text{s}$ for 3.5 kHz link) after the recovering diodes have stopped conducting. Standard reverse recovery only occurs when the converter is boosting voltage from input to output, and then occurs at very low di/dt with the link capacitance buffering the reverse voltage drop after the diode starts blocking reverse voltage.

B. Parasitic Inductance Losses

Parasitic inductance losses occur due to the inductance of the line and link capacitors, the switch module, and connecting circuitry. Very low inductance laminated bus bars, low inductance modules, and low inductance capacitors minimize this loss, given by:

$$\begin{aligned} P_{ind} &= f_L * 8 * 0.5 * L_{stray} * I_p^2 \\ &= f_L * 8 * 0.5 * 30 \text{ nH} * 2800^2 \\ &= 3.28 \text{ kW} (0.163\%) \end{aligned} \quad (3)$$

where L_{stray} is the estimated stray inductance referred to each switch. The factor of 8 is an approximation for the number of stray loss events that occur in each link cycle.

C. Turn off transition losses

Tests are planned for Punch Through (PT) IGBTs to measure the exact losses during the switch turn-offs. Preliminary test results for non-PT (NPT) IGBTs are below, but modeling results suggest that PT IGBTs have much lower soft turn-off losses compared with NPT IGBTs. Until those PT results are available, (3) and (4) from [15] are solved for both hard and soft turn-off, with parameters chosen to match the V-I waveforms and turn-off losses reported for high power PT, ABB IGBTs (6500 V, 600 A). The resulting hard turn-off waveform to match the data sheet turn-off energy of 3.15 J at 125 °C is shown in Figure 5.

When the equations are applied to soft turn-off, under the conditions stated above for the 2MW, 2300V converter, the current and voltage shown in Figure 6, “10% Ramp Time”, occur, with only 180 mJ loss despite having about 4 times higher current at turn-off. Ramp Time is the time required for the switch voltage to reach nominal link voltage, and may be expressed as a percentage of the nominal link charging time. A 10% ramp time is 5% of the link cycle time. For comparison, the I-V waveforms for a 2% ramp time case is also shown. Hence very little current flows through the switches at turn-off, and the little current that does flow does so over a low voltage and decays to near zero before the voltage rises much, resulting in very low turn-off losses of only 0.18% (4) of the converter power, even at the effective switching frequency of 7 kHz.

An indication of the validity of this soft turn-off model is to compare its behavior to a physical device simulation based on solving the Poisson’s equations for a two dimensionally described IGBT, as implemented in Silvaco Inc’s Atlas. Using a physical IGBT model already present in the Atlas example library, a 60A inductive soft turn-off into a 300 volt bus, with a 0.35 μF “snubber” capacitor across the IGBT was simulated. The PT IGBT had a carrier lifetime of 100 ns. After selecting the model parameters to best match the simulation results, the current and voltage curves at turn-off were a near perfect match to the simulation, as shown in Figure 7. Total turn-off losses are then –

$$\begin{aligned} P_{turn\text{off}} &= f_L * 6 * E_{turn} \\ &= 3500 * 6 * 0.18 \text{ J} \\ &= 3.78 \text{ kW} (0.18\%) \end{aligned} \quad (4)$$

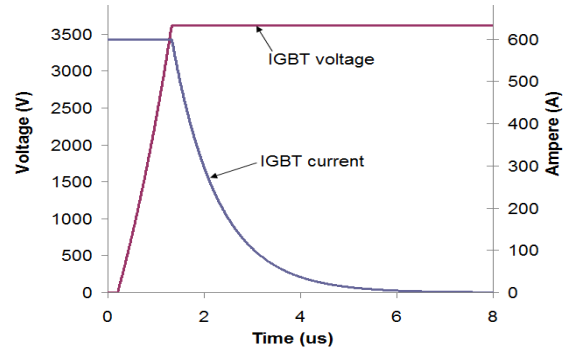


Figure 5. Hard turn-off of the 6500V, 600A ABB IGBT – by equations

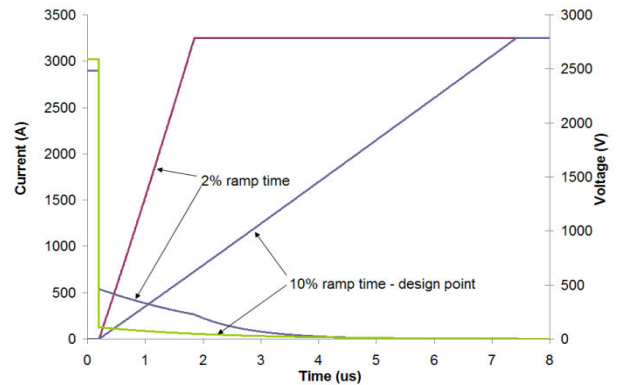


Figure 6. Soft turn-off of the 6500V, 600A ABB IGBT – by equations

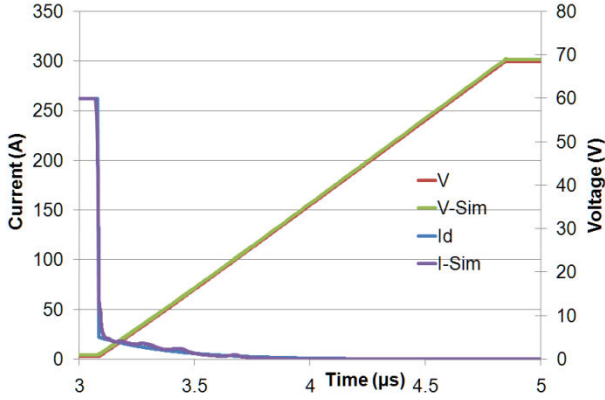


Figure 7. Match of model to Simulation

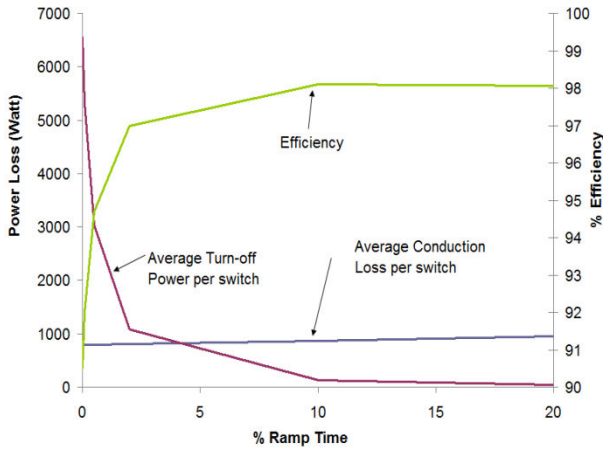


Figure 8. Optimizing Ramp Time

Since turn-off losses decrease with increasing link capacitance and the corresponding increase of ramp time, but peak link current and power throughput decrease with increasing link capacitance, an optimum link capacitance for a given link frequency must be chosen. Figure 8 shows that turn-off losses fall rapidly with increasing ramp time, while conduction losses increase slowly. In this case, the optimum efficiency of 98% is nominally at 10 % ramp time.

Link losses are primarily due to the ac resistance of the inductor, as the air core has no core losses other than a small amount due to leakage flux between the toroidally arranged coils. Due to the use of type 8 Litz wire on a simple, spiral wound coil, the ac resistance is negligibly higher than the dc resistance, and with 70% copper fraction, the coil has a relatively low resistance. The Inductance to Resistance ratio (L/R) of each coil, along with the link frequency, determines the efficiency of the link inductor. The L/R depends on the geometry of the coils, with larger coils having a higher L/R. The L/R of the 15 kW prototype is 200 $\mu\text{H}/20 \text{ m}\Omega$, and results in 0.5% total loss when operated at 7 kHz link frequency. Doubling the diameter doubles the L/R, which maintains the 0.5% total loss number when the link frequency is reduced to 3.5 kHz as it is for the 2 MW medium voltage converter examined here. With an L/R, then, of 400 $\mu\text{H}/20 \text{ m}\Omega$, and a total inductance of 75 μH , the resistance of the medium voltage link inductor is only 4.5 m Ω , so the loss is:

$$P_{link} = (1 - 0.05) * 0.0045\Omega * (0.577 * 2800)^2 = 11131 \text{ W (0.55\%)} \quad (5)$$

IV. SIMULATION RESULTS

PSIM Simulations were carried out for a 2MW, 2300 V converter using the above mentioned configuration. The link frequency chosen was 3.5 kHz. The schematic used for simulation is shown in Figure 12.

Figure 9 and Figure 10 show the input currents and voltages for full power operation with equal input and output voltages, while Figure 11 and Figure 13 show the link current and voltage for the same case. It can be seen that the input currents are highly sinusoidal with very low harmonics. Calculations on the input currents results in a highly acceptable THD of 1.38% below the 7 kHz ripple frequency, and a ripple magnitude that contributes an additional 1% THD, for less than 2.5% total THD. It is believed that slight imperfections in the switching control are responsible for the distortion below 7 kHz, and that further work can mostly eliminate these very low amplitude harmonics. Figure 14 and Figure 15 show converter and link currents and voltages for output references at half the input frequency.

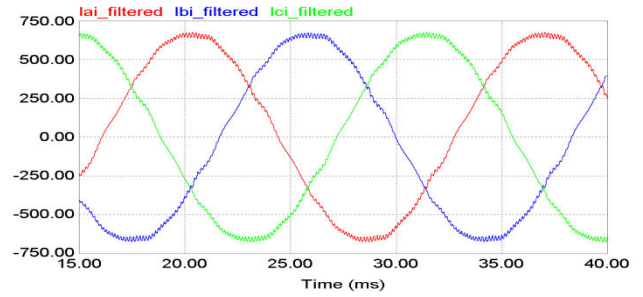


Figure 9. Input currents during full power operation

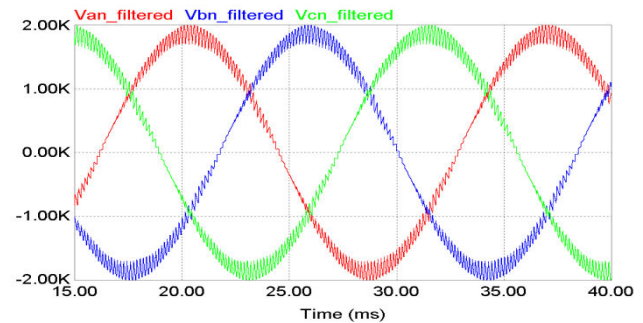


Figure 10. Phase voltages at input during full power operation

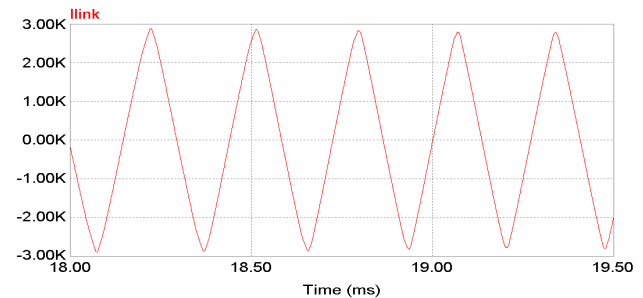


Figure 11. Link current during full power operation

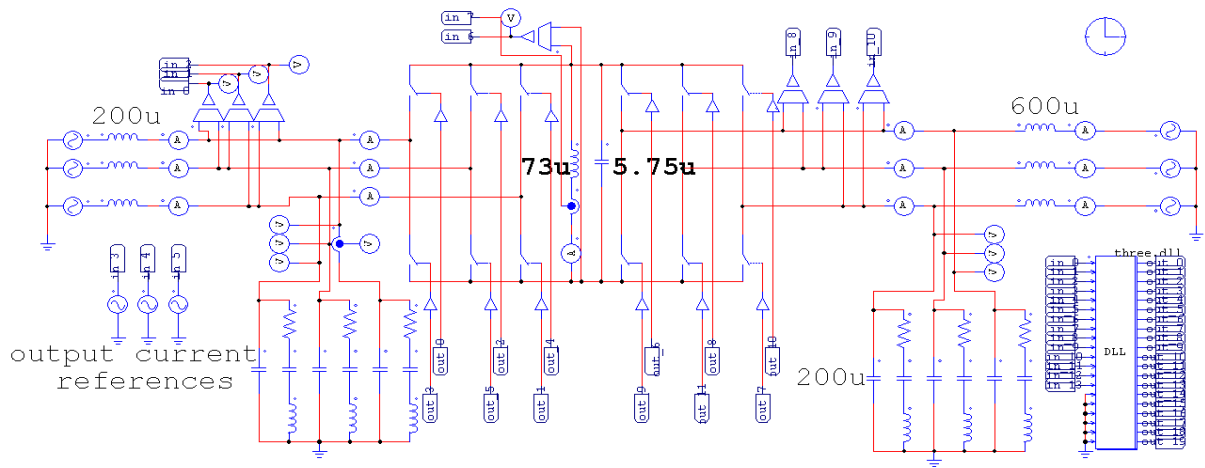


Figure 12. PSIM schematic used for simulation

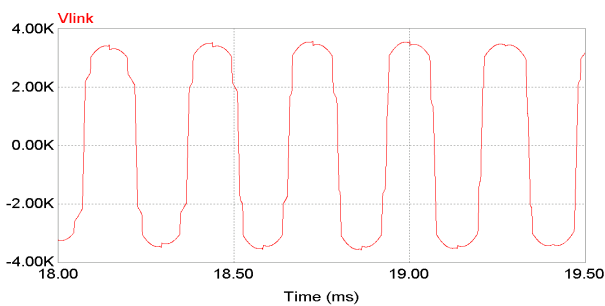


Figure 13. Link voltage during full power operation

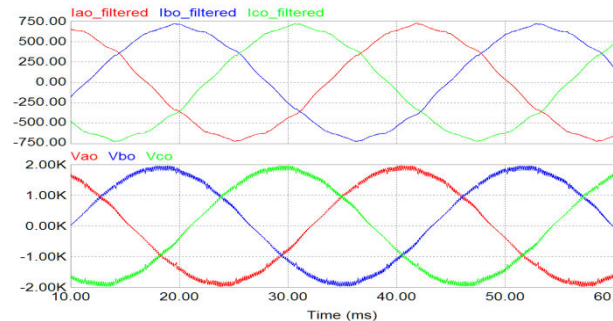


Figure 14. Output current and voltage with reference output at full power at 30 Hz

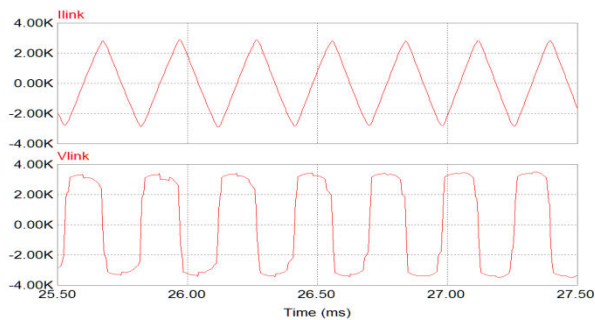


Figure 15. Link current and voltage during 30 Hz operation

V. REDUCED POWER AND VOLTAGE OPERATION

Power and current throughput is controlled by the amount of charge delivered by the link on each cycle, as by reducing the current pulse widths shown in Figure 4.

Reducing the charge in each “on” mode reduces the power throughput, and increases the link frequency. As power approaches zero, the link waveform becomes sinusoidal, at roughly 2 to 3 times the full power link frequency (depending on the link capacitance).

High ratios of buck or boost, such as full current operation into zero voltage and/or power factor are accommodated by fully charging the link from the input, then discharging to the output, and since there is no power transfer to the output, the link energy is then returned to the input. This technique may also be used to transfer full current from a zero voltage and/or power factor input to a full voltage output, with of course no power actually going to the output in that case. A 6-switch version of this topology may be used to do nothing more than active reactive compensation, acting as a continuously variable capacitance or inductance on a three phase line.

VI. PRELIMINARY PROTOTYPE RESULTS

The 15 kW “proof-of-principle” prototype shown in Figure 18 and Figure 19 uses 24, 1000 V, 60A rated NPT IGBTs with diodes to form the 12 ac switches needed for its three-phase ac to three-phase ac operation. Low level control is through an FPGA programmed in AHDL with circuit sensing provided by 8, 3 MBPS, 12 bit, ADCs. Three 20 μ F film capacitors are connected line-to-line across each of the input and output lines. The link inductor is a spiral wound coil of Type 8 Litz wire with a dc resistance of 15 m Ω , and inductance of 100 μ H, and a free-air Q-factor of 125. When placed in the ferrite C-core shielded link inductor assembly, the inductance rises to about 190 μ H, as determined by the measured 6400 Hz link frequency, the 600V average peak link voltage, and the 120A peak current as measured by the dV/dt on the 0.3 μ F link capacitance during the partial resonance period (Figure 16).

Figure 16 below shows the converter running in a simple test as a self-powered dc-dc converter, running off only the energy in the input line capacitors charged to 600 volts. Converter operation was terminated after 10 power cycles (5 link cycles), at the 900 μ s mark. From the know link inductance, voltage, and frequency, the link

current may be estimated at 120 amps peak, which is supported by the dV/dt at turnoff shown in Figure 16 of 400 V/ μ s. Each switch sees $\frac{1}{2}$ of this, or 200 V/ μ s. The resulting power level is 17 kW. Efficiency may be estimated from the voltage drop of the link over the 10 power cycles, and is computed at 93%. The loss model at this power level predicts 95.4% efficiency, with an assumed turn-off loss, so there is apparently about 2.4% of additional unaccounted for losses. These may be from excessively long IGBT tail current, as some IGBTs have that characteristic, or the loss could be from one or more of the other converter components. The data sheet for this IGBT does not give its turn-off loss, and we have no model for its soft turn-off loss.

Testing will soon be conducted at sustained full power dc-dc that may indicate where these excessive losses occur. Converter output will be routed back to the input, with that dc current being measured, and compared with the dc current coming from an external power supply which will make up the converter losses, which will give an accurate indication of converter efficiency. Detailed turn-off testing of the prototype IGBTs to determine their turn-off losses are to be carried out. Earlier tests of the shielded link inductor showed no sign of core saturation with this large air gap inductor, so excessive core loss seems unlikely. Stray inductance, as calculated from the small amplitude link ringing after switch turn-on is calculated as 360 nH, which, while a bit high, accounts for only 0.4% of total power, and is included in the 95.4% efficiency prediction.



Figure 18. 15 kW prototype



Figure 19. Link inductor

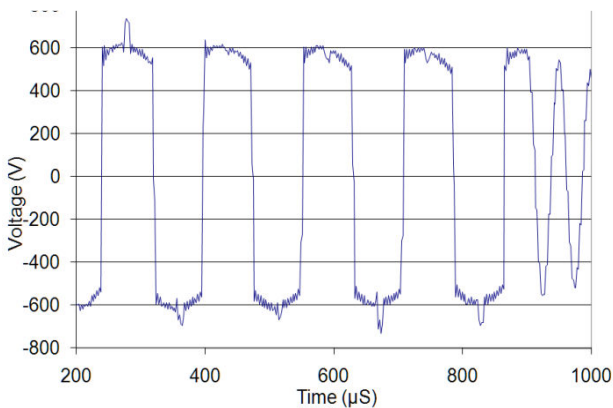


Figure 16. Link voltage in 15 kW prototype

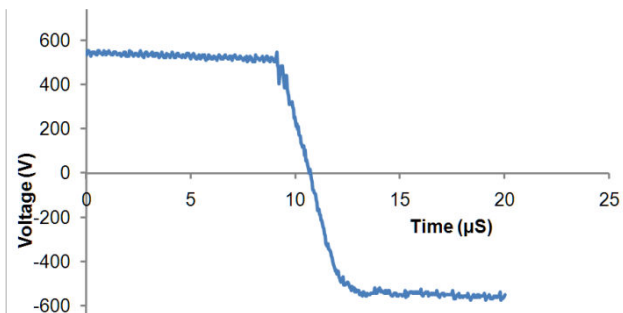


Figure 17. Source capacitance voltage during efficiency test on prototype

VII. OTHER EFFICIENCY PREDICTION AND TEST RESULTS

Modeling with SIMplorer was done on an available IGBT model, the NPT, IRG6S60b120, a 1200 V, 60 A rated device with a diode. As shown in Figure 20, turn-off loss at 100 A and 650 V, with a 0.55 μ F link capacitor was found to be 1.43 mJ. When used on a 15 kW 460 Vac converter, as with the 15 kW prototype, the turn-off loss for this device is 0.34% of the total power. If used in the prototype configuration, this device produces a converter efficiency of 95.5%.

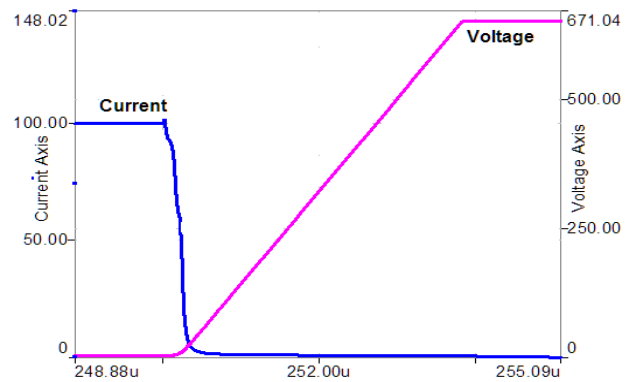


Figure 20. Turn off simulation in SIMplorer

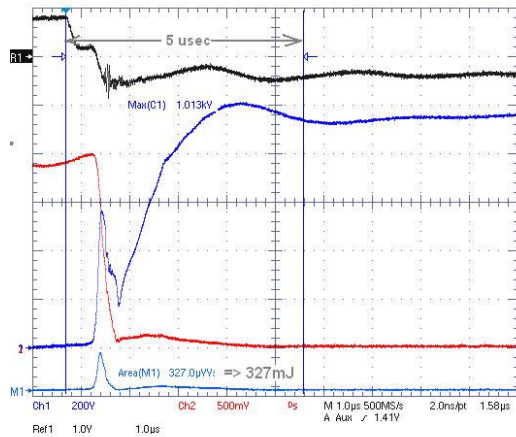


Figure 21. Real device turn-off waveforms

Experiments were conducted at the laboratory of F.L. Rees & Associates, Inc on a high powered NPT IGBT (*CM1000DU-34NF*) at 1000 V, 2000 A, with a 3.3 μF capacitor connected across the collector and emitter to simulate a link capacitor. Although this capacitance was less than half what the actual link capacitor would be with this device, and the stray capacitance at 80 nH was more than double the stray capacitance that a well constructed converter would have, the total turn-off loss was 327 mJ. About 50% of this was due to the stray inductance, with turn-off waveforms shown in Figure 20. This total turn-off loss corresponds to 1% of the converter power of 475 kW with a 3500 Hz link frequency. The loss model with this device and measured turn-off loss indicates a full power efficiency of 97% with a 3 kHz link

Note that the current during the voltage rise does not decay, only falling with decreased du/dt , possibly due to the very long carrier lifetime ($> 10 \mu\text{s}$) of NPT devices. As per the above simulation and modeling results for PT IGBTs, we anticipate significantly reduced soft turn-off losses for those devices due to their much shorter carrier lifetime ($< 0.5 \mu\text{s}$).

VIII. COMPONENT SELECTION

Component selection for a given application involves a number of tradeoffs regarding costs, size, weight, and efficiency, with optimum points largely dependent on voltage and power levels. Choice of link frequency is a tradeoff between link inductor size, its losses, and switching losses as given by turn-off and stray inductance losses. Lower link frequency produces lower switching losses, but will have higher link losses, unless a larger, more efficient link inductor is used.

Link frequency, in conjunction with line filter capacitance, determines the required line inductance. The resonant frequency of the line inductance and capacitance must be less than twice the link frequency.

The PSIM simulation was run with passive damping, but further controls development is anticipated to utilize active damping, taking advantage of the flexible charge control possible with this topology. This will eliminate those components and the small associated loss.

IX. CONCLUSION

The Soft Switched Ac-Link Buck-Boost Converter may be utilized in a wide variety of applications ranging from low and medium voltage motor drives, to transformer-less solar inverters, large wind power converters, isolated ac-dc bi-directional converters, and many other applications that may benefit from its conversion versatility, soft-switching efficiency, input-output isolation, and high power quality. The topology is expected to offer relatively low cost, low weight, compact and efficient power converters and motor drives

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